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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,416	11/16/2001	Ta-Lee Yu	B-4392 619330-6	5531

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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,416	YU ET AL.	
	Examiner	Art Unit	
	Quang D. Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,7-12 and 14-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-12 and 14-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 7-12 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,465,189 to Polgreen et al. in view of US Patent No. 6,621,133 to Chen et al.

Regarding claim 1, Polgreen et al. (figures 8-29) teach a low voltage triggered electrostatic discharge (LVTESD) protection circuit, coupled to a pad of an integrated circuit to protect core circuits of the IC from ESD event, the ESD protection circuit comprising:

a semiconductor substrate having the first conductivity type (p-type);

an well region (n well) having the second conductivity type (n-type), formed in the semiconductor substrate;

an anode doped region (p type anode) having the first conductivity type (p-type), formed in the well region (n well);

a gate structure (39), formed in the semiconductor substrate and outside the well region (n well), the gate structure (39) having a first side (right side of gate [39]) and a second side (left side of gate [39]);

a first doped region (n-type doped region is formed on the right side of the gate [39]) having the second conductivity type (n-type), formed between the well region (n well) and the gate structure (39), immediately adjacent to the first side (right side of the gate [39]) of the gate structure (39) in the semiconductor substrate; and

a second doped region (n-type doped region is formed on the left side of the gate [39]) having the second conductivity type (n-type), formed next to the second side (left side of the gate [39]) of the gate structure (39) in the semiconductor substrate, wherein the first doped region (n-type doped region is formed on the right side of the gate [39]) and the second doped region (n-type doped region is formed on the left side of the gate [39]) are heavily doped regions (n+ type).

Polgreen et al. differ from the claimed invention by not showing a plurality of isolated islands distributed in the first doped region so that the resistance of the first doped region is increased, wherein at least one of the isolated islands is completely surrounded by the first doped region. However, Chen et al. (figures 5-7) teach a plurality of isolated islands (32a) distributed in the first doped region (22) having the second conductivity type (n+ type), wherein at least one of the isolated islands (32a) is completely surrounded by the first doped region (22) (figure 5). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Chen et al. into the device taught by Polgreen et al. because it increases the resistivity of the diffusion areas.

Regarding claim 2, the combined device shows a first contact region (Polgreen et al.; p-type contact region) having the first conductivity type (p-type), formed in the semiconductor substrate;

a second contact region (Polgreen et al.; n-type contact region) having the second conductivity type (n-type), formed in the well region (Polgreen et al.; n well); and

the first contact region (Polgreen et al.; p-type contact region) is coupled to the second doped region (Polgreen et al.; n-type doped region is on the left side of the gate [39]) and a power pad (Polgreen et al.; Vss) of the integrated circuit, and the anode doped region (Polgreen et al.; p-type anode region) is coupled to the pad.

Regarding claim 3, the combined device shows the second contact region (Polgreen et al.; n-type contact region) is coupled to the anode doped region (Polgreen et al.; p-type anode region).

Regarding claim 7, the combined device shows the isolated islands are field oxide (Chen et al.; 32a).

Regarding claim 8, the combined device shows each of the isolated islands (Chen et al.; 32a) has approximately the same width.

Regarding claim 9, the combined device shows each of the isolated islands (Chen et al.; 32a) is elongated and approximately parallel to the first side of the gate structure.

Regarding claim 10, the combined device shows each of the isolated islands (Chen et al.; 32a) is elongated and approximately perpendicular to the first side of the gate structure.

Regarding claim 11, the combined device shows the first conductivity type is a p-type (Polgreen et al.; p-type), and the second conductivity type is an n-type (Polgreen et al.; n-type).

Regarding claim 12, Polgreen et al. (figures 8-29) teach a low voltage triggered electrostatic discharge (LVTESD) protection circuit, coupled to a pad of an integrated circuit to protect core circuits of the IC from ESD event, the LVTESD protection circuit comprising:

a semiconductor control rectifier, comprising an anode (an anode is a node portion, which is a connection between the PAD and the p-type region), a anode gate (n well), a cathode (a cathode is a node portion, which is a connection between the Vss and the n-type region) and a cathode gate (p-type substrate), the anode (an anode is a node portion, which is a connection between the PAD and the p-type region) is coupled to the pad (PAD); and

a MOS having a second conductivity type (n-type), formed on a semiconductor substrate having a first conductivity type (p-type) comprising a well (n well) having the second conductivity type (n-type), the MOS comprising:

a gate structure (39), formed in the semiconductor substrate, having a first side (right side of gate [39]) and a second side (left side of gate [39]);

a first doped region (n-type doped region is formed on the right side of the gate [39]), formed in the semiconductor substrate between the well region (n well) and the gate structure (39) and immediately adjacent to the first side (right side of the gate [39]) of the gate structure (39), comprising at least one contact region (a portion of the n region) coupled to the anode gate (n well); and

a second doped region (n-type doped region is formed on the left side of the gate [39]), formed in the semiconductor substrate to the second side (left side of the gate [39]) of the gate structure (39) in the semiconductor substrate, and coupled to the cathode (a cathode is a node portion, which is a connection between the Vss and the n-type region), wherein the first doped region (n-type doped region is formed on the right side of the gate [39]) and the second doped region (n-type doped region is formed on the left side of the gate [39]) are heavily doped regions (n+ type).

Polgreen et al. differ from the claimed invention by not showing a plurality of isolated islands distributed in the first doped region so that the resistance of the first doped region is increased, wherein at least one of the isolated islands is completely surrounded by the first doped region. However, Chen et al. (figures 5-7) teach a plurality of isolated islands (32a) distributed in the first doped region (22) having the second conductivity type (n+ type), wherein at least one of the isolated islands (32a) is completely surrounded by the first doped region (22) (figure 5). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Chen et al. into the device taught by Polgreen et al. because it increases the resistivity of the diffusion areas.

Regarding claim 14, the combined device shows a plurality of oxide layers, and each of the isolated islands (Chen et al.; 32a) is formed by one of the oxide layers.

Regarding claim 15, the combined device shows each of the isolated islands (Chen et al.; 32a) has approximately the same length.

Regarding claim 16, the combined device shows each of the isolated islands (Chen et al.; 32a) has an elongated profile and is approximately parallel to the first side of the gate structure.

Regarding claim 17, the combined device shows each of the isolated islands (Chen et al.; 32a) has an elongated profile and is approximately perpendicular to the first side of the gate structure.

Regarding claim 18, the combined device shows the first conductivity type is a p-type (Polgreen et al.; p-type), and the second conductivity type is an n-type (Polgreen et al.; n-type).

Response to Arguments

Applicant's arguments filed 02/01/05 have been fully considered but they are not persuasive.

It is argued, in page 2 of the remarks, that Polgreen et al. and Chen et al. teach or suggest the identical base resistance values in parasitic transistors through symmetrical design, so the resistance of the doped region is not increased. This argument is not convincing because the applicant fails to include the identical base resistance values in parasitic transistors through symmetrical design in the claimed limitations of claim 1. However, the combined device (Polgreen et al. and Chen et al.) teaches the claimed limitations of claim 1, including a plurality of isolated islands distributed in the first doped region so that the resistance of the first doped region is increased.

It is argued, in page 3 of the remarks, that Polgreen et al. and Chen et al. teach or suggest a first side contact with first doped region and a second side contact with another doped region, so the island is not completely surrounded by the first doped region. This argument is not convincing because the applicant fails to include a first side contact with first doped region and a second side contact with another doped region in the claimed limitations of claim 1. However, the combined device (Polgreen et al. and Chen et al.) teaches the claimed limitations of claim 1, including the isolated islands is completely surrounded by the first doped region.

It is agued, in page 3 of the remarks, that Polgreen et al. and Chen et al. do not teach or suggest at least one of the isolated islands is completely surrounded by the first doped region. This argument is not convincing because the combined device (Polgreen et al. and Chen et al.)

teaches the claimed limitations of claim 12, including at least one of the isolated islands is completely surrounded by the first doped region.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D. Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
June 7, 2005

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